PHYSICAL LIMITS FOR SCALING OF INTREGRATED CIRCUITS

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In this paper we discuss some physical limits for scaling of devices and conducting paths inside of semiconductor integrated circuits (ICs). Since 40 years only a semiconductor technology, mostly the CMOS and the TTL technologies, are used for fabrication of integrated circuits in the industrial scale. Miniaturization of electronic devices in integrated circuits has technological limits and physical limits as well. In 2010 best parameters of commercial ICs shown the dual-core Intel Core i5-670 processor manufactured in the technology of 32 nm. Its clock frequency in turbo mode is 3.73 GHz. A forecast of the development of the semiconductor industry (ITRS 2009) predicts that sizes of electronic devices in ICs circuits will be smaller than 10 nm in the next 10 years. The physical gate length in a MOSFET will even amount 7 nm in the year 2024. At least 5 physical effects should be taken into account if we discuss limits of scaling of integrated circuits.

1. Quantization of both electrical and thermal conductance in narrow and thin transistors` channels and in conducting paths.

2. Spread of doping atoms in a semiconductor material. In a n-doped silicon cube with the size of $(10\ \text{nm})^3$ there are 5×10^4 atoms and 1% chance only to find one free electron. In order to keep the conductive properties of the semiconductor material one should apply more intensive doping, eg. $10^{20}\ \text{cm}^{-3}$. Low number of free electrons should be scattered evenly in whole volume of a material.

3. Electrostatics; a loss of electrostatic control of the drain current in a MOSFET. The channel length L_E of Si MOSFET is limited by a degradation of electrostatic control in the transistor. The minimal channel length depends on thickness of channel H_{ch}, thickness of insulation layer H_i, dielectric constants of a channel ε and insulation ε_i . If we take the ratio $\varepsilon_i/\varepsilon \approx 0.3$ (for silicon oxide and silicon), thickness of channel $H_{ch} = 2$ nm, thickness of insulation $H_i = 1.5$ nm – the estimated minimal length of channel is $L_E \approx 3$ nm.

4. Electron tunneling between a source and a drain inside a MOSFET through a insulation (oxide). The tunneling effect depends on the channel length L and the supply voltage (drain-source voltage).

5. Propagation time of electromagnetic wave along and across a chip (IC); The new quad-core Intel Core i5-670 processor has a width $a = 37.5$ mm and a length $b = 37.5$ mm. The period of the highest clock frequency (3.73 GHz) is $T_{ck} = 270$ ps. But the propagation time for an electromagnetic wave across a chip is $T_p = = 300$ ps. According to the state of the art the minimal length of gate in MOSFET in silicon integrated circuits is around 3 nm (thus – technology of 3 nm!). However technological limits allow to apply only the 10 nm-technology in the next 10 years.